REMARKS

Claims 1-21 are pending in the current application. Claims 1, 12 and 16 are independent claims. Favorable reconsideration and withdrawal of the rejection is respectfully requested in view of the following remarks.

EXAMPLE EMBODIMENTS OF THE PRESENT INVENTION

Example embodiments of the present invention provide "...a multi-chip semiconductor package having stacked semiconductor package structures, each [package structure] of which includes a **substrate**; a semiconductor chip which is electrically mounted in a predetermined portion of the substrate; **an enclosure body covering the entire surface of the substrate** where the semiconductor chip is mounted; **a plurality of conductive studs formed through the enclosure body** on both sides of the semiconductor chip; and conductive members, such as solder balls or conductive patterns, provided on the bottom of the substrate in contact with each of the conductive studs." Specification, paragraph [0011] (emphasis added).

35 U.S.C. § 103 (a) REJECTION – LONDA AND MOSTAFAZADEH

Claims 1-21 remain rejected under 35 U.S.C. § 103(a) as unpatentable over Londa, U.S. Patent No. 6,101,100, in view of Mostafazadeh et al. (hereinafter "Mostafazadeh"), U.S. Patent No. 5,783,870. Applicant respectfully traverses this rejection.

Each of the independent claims 1, 12 and 16 recite conductive studs that **extend through the enclosure body** outside a periphery of the semiconductor chip. Example, non-limiting embodiments of this feature are discussed throughout the Specification. The Examiner's attention is respectfully directed, for example, to paragraphs [0029]-[0031].

Applicant submits that Londa in view of Mostafazadeh fails to teach or suggest the **conductive studs extending through the enclosure body** outside a periphery of the semiconductor chip as taught by example embodiments of the claimed invention.

Londa

In the *Response to Arguments* section of the Office Action, the Examiner asserts "[c]onductive studs (42, 44, 46) extend through the **first and second substrates** (12, 22) to electrically couple circuitry layers (20, 27), and since the circuitry layers are on the outside surfaces of the chip, the conductive studs must be outside a periphery of the chip in order to electrically couple the two circuitry layers." Action, p. 2.

Applicants agree with the Examiner that Londa teaches the conductive studs **extend through the substrate**. However, Applicants respectfully point out to the Examiner that independent claims 1 and 12 of the present application recite "a plurality of conductive studs extending through **the enclosure body**," not extending through the substrate. Londa explicitly teaches "...a plurality of plated **through holes 42, 44, 46, 48, 50, 52 extending through first and second substrates 12, 22** and plane 30 for electrically coupling first and second layers of circuitry 20, 27." Londa, col. 4, lines 15-29 (emphasis added). Applicants submit that the substrates 12, 22 fail to read upon the enclosure body, recited in independent claims 1 and 12, for at least the reasons given below.

Applicants submit that the structure shown in Fig. 2 of Londa is merely conventional art as discussed in paragraphs [0005] – [0009] of the present application wherein a) the semiconductor devices 36,40 may be bonded to conductive pads or a pattern (not shown) of the substrates 12,22 by means of a wire 102, b) a plurality of through holes 42,44,46, which provide interlayer connecting paths, are formed through substrates 12,22 outside the periphery of the encapulsant 104, c) the plurality of through holes 42,44,46 are spaced from the encapulsant 104 by a predetermined distance in order to insulate them from the semiconductor chip 40' of the other package structure, and d) because the plurality of through holes 42,44,46 penetrate the substrate 12,22, the plurality of through holes 42,44,46 must be separated and insulated from the encapulsant 104.

Thus, when the through holes 42,44,46 extend through the substrate (as explicitly taught by Londa), the plurality of through holes 42,44,46 are spaced away from the encapsulant 104 in order to insulate the semiconductor chips 36 and 40 of package 10 from the semiconductor chips 40' of the package 10'.

Furthermore, the substrates 12,22 fail to read upon the enclosure body, as recited in independent claims 1 and 12, at least by the Examiner's acknowledgement that "...Londa does not disclose expressly wherein the multi-chip has an enclosure body covering substantially the entire upper surface of the substrate." Action, p. 4.

Mostafazadeh

On the other hand, Mostafazadeh fails to teach that a die 46 is connected to a substrate. Mostafazadeh states "[a]n integrated circuit die 46 is also illustrated **within** package 32, where terminals of die 46 are **connected, using wires, traces, and vias, to pads 40 and 54**." Mostafazadeh, col. 4, lines 6-8 (emphasis added). Because the die 46 is not connected to a substrate, insulation of the conductive via 43 from the die 46 is not necessary. Therefore, the die 46 may be formed within the package 32 (which the Examiner believes reads on the enclosure body recited in independent claims 1 and 12) and the conductive via 43 may extend through the package 32.

Combination of Londa and Mostafazadeh

In an attempt to provide motivation to combine Londa and Mostafazadeh, the Examiner asserts "[t]he motivation for extending the holes 42/44/46 comes from the need to maintain electrical contact between adjacent semiconductor chips." Action, p. 3.

Applicants submit that Mostafazadeh and Londa teach two different methods for electrically connecting the semiconductor devices wherein the methods that cannot be combined without defeating or profoundly altering the intended purpose of the other reference, at least for similar reasons as discussed above with regard to the conventional art. Specifically, because the through holes 42,44,46 of Londa extend through the substrate 12,22, the package 32 of Mostafazadeh (wherein the conductive vias 43 extend through the package 32) may not combine with the teaching of Londa such that the electronic devices 36,40 of package 10 would be insulated from the electronic device 40' of package 10'.

Furthermore, Applicants appreciate the Examiner's attempt to particularly point out a teaching in the reference to support the rejection. However, proper evidence of motivation that would lead one of ordinary skill in the art to combine the teachings of Londa and Mostafazadeh has not been supplied. "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'. In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999). "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight." In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed.Cir. 1999).

Specifically, the alleged motivation is not present in Londa or Mostafazadeh. The motivation has merely been alleged by the Examiner based upon Applicants' invention, in an impermissible hindsight reconstruction. The Examiner has used the present application as a blueprint, selected Londa relating to a stacked package structure and relied on Mostafazadeh to supply the missing elements without identifying any **specific** evidence of motivation to combine motivation and obviousness, other than providing conclusory statements regarding the knowledge in the art.

Thus, Applicant submits that Londa in view of Mostafazadeh fails to teach or suggest "a plurality of conductive studs extending through the enclosure body outside a periphery of the semiconductor chip" as recited in independent claims 1 and 12.

In view of the above arguments, Applicant submits that Londa in view of Mostafazadeh also fails to teach or suggest "forming an enclosure body encapsulating the upper surface of the substrate, the semiconductor chip and the conductive studs" as recited in independent claim 16.

Reconsideration and withdrawal of the rejection to independent claims 1, 12, 16 and claims 2-11, 13-15 and 17-21, at least by virtue of their dependency on independent claims 1, 12 and 16, respectively, is kindly requested.

CONCLUSION

Accordingly, in view of the above, reconsideration of the objections and rejections and allowance of each of claims 1-21 in connection with the present application is earnestly solicited.

Should there be any matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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